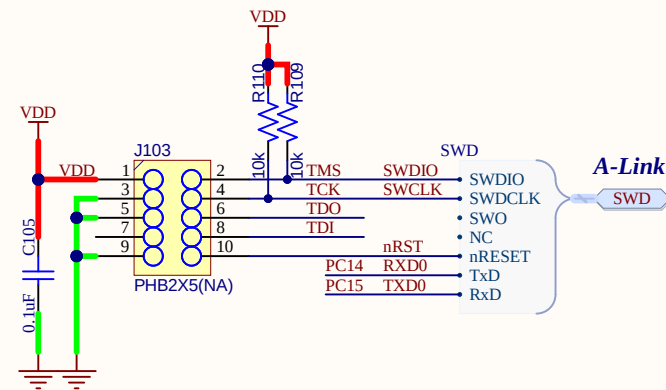


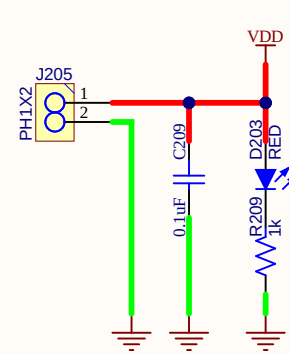
We recommend using X-tal Load capacitor value.

CLOCK

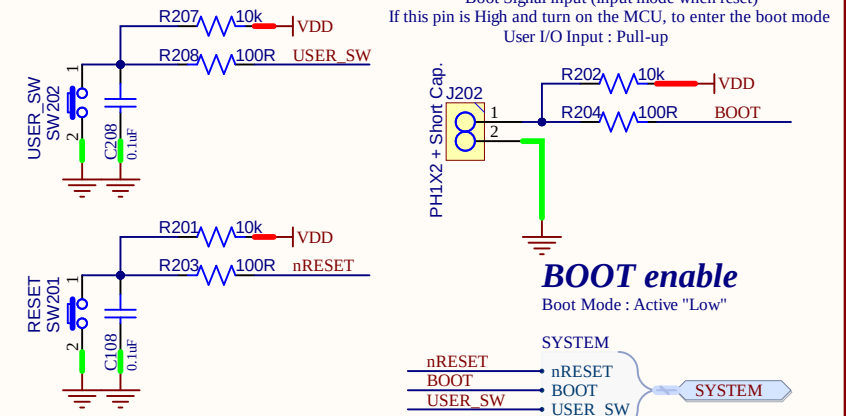


(SWCLK-Pull up, SWDIO-Pull up)

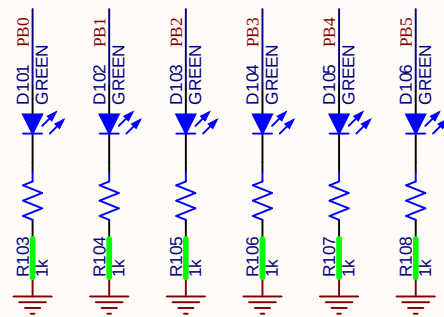
Cortex Debug Connector (SWD)



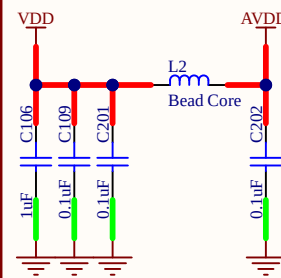
POWER



▲ C204 : Remove when using as user I/O port

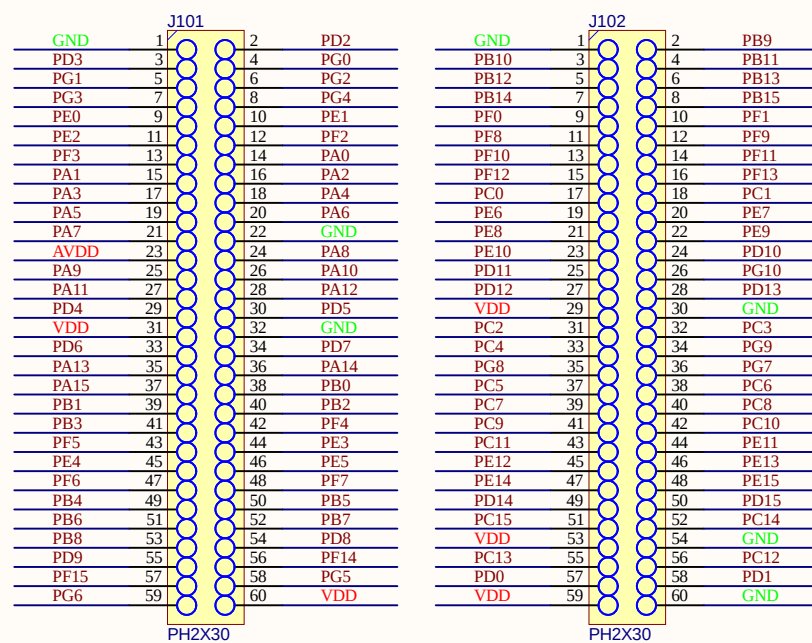
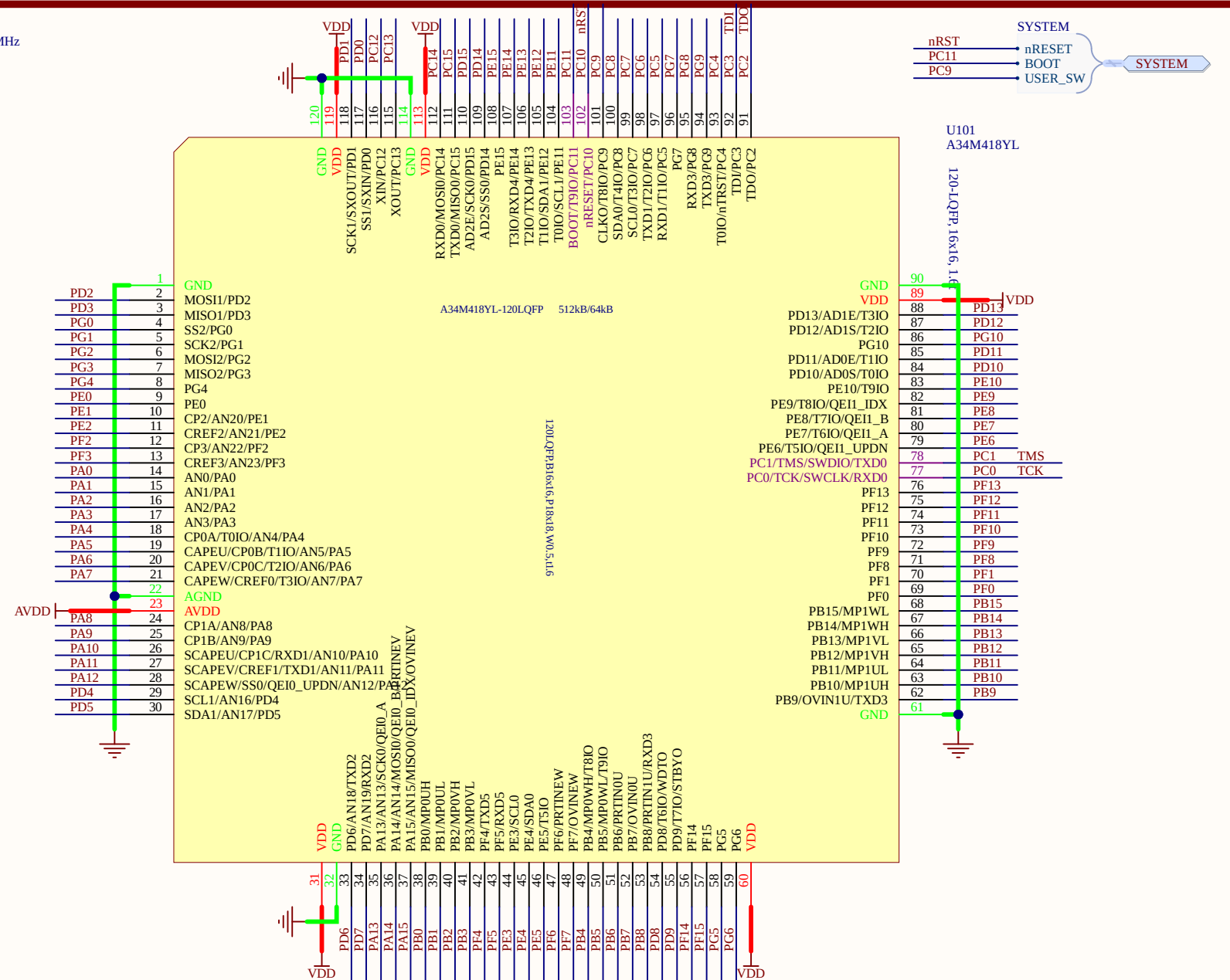


PWM LED

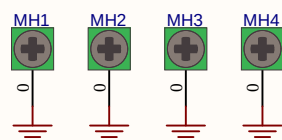


Bypass Cap.

JTAG (O) / SWD (O)
PLL Clock : 8MHz~120MHz



USER IO



MOUNTING HOLE

