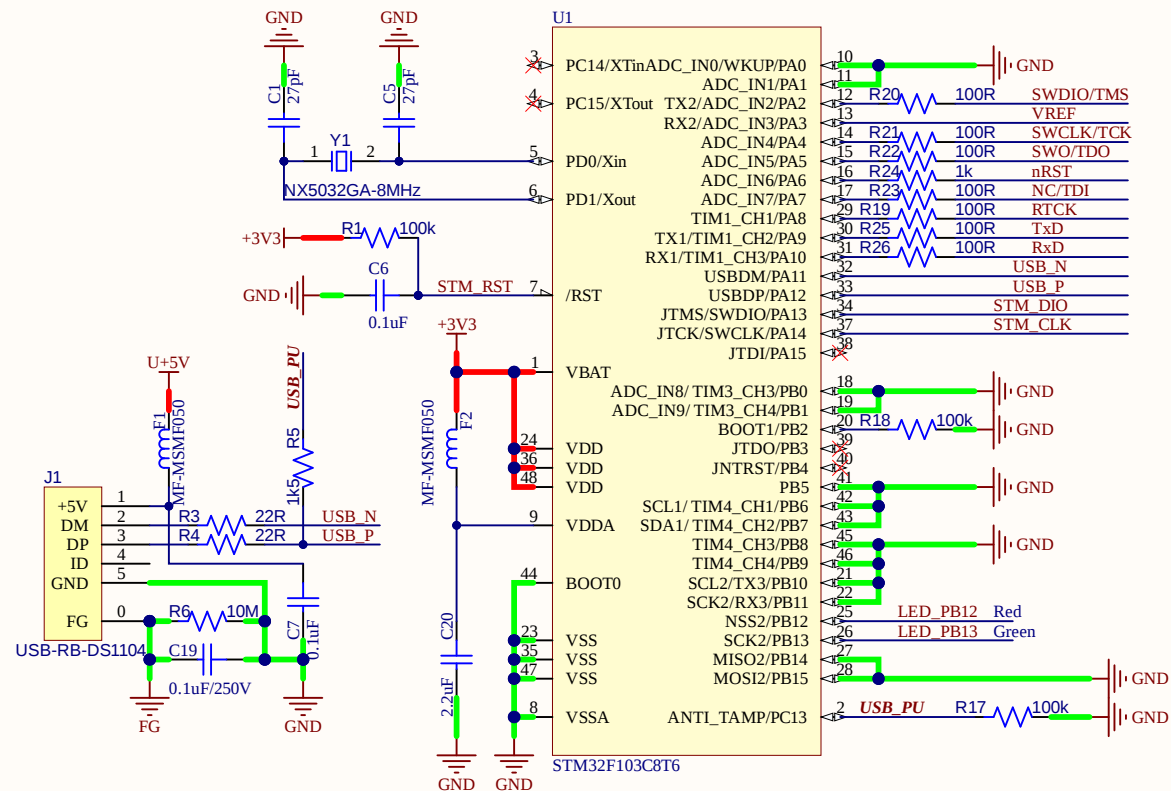
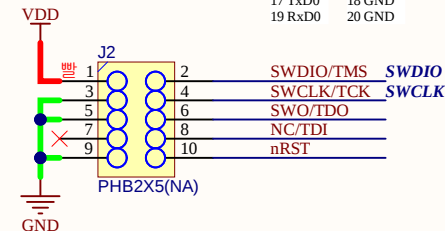


Cortex Debug Connector

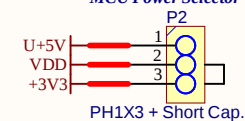
|             |              |
|-------------|--------------|
| 1 VCC       | 2 SWDIO/TMS  |
| 3 GND       | 4 SWDCLK/TCK |
| 5 GND       | 6 SWO/TDO    |
| 7 NC        | 8 NC/TDI     |
| 9 GNDDetect | 10 nRESET    |

JTAG 20Pin Connector

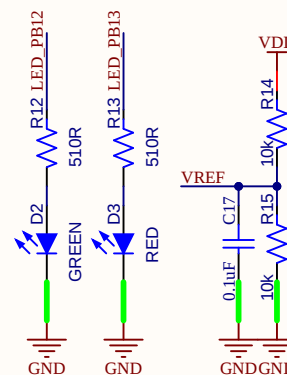
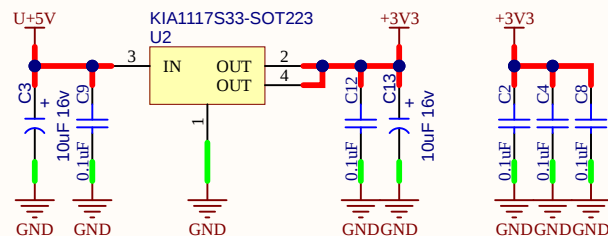
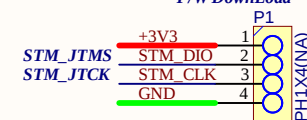
|         |        |
|---------|--------|
| 1 Vref  | 2 NC   |
| 3 nTRST | 4 GND  |
| 5 TMI   | 6 GND  |
| 7 TMS   | 8 GND  |
| 9 TCK   | 10 GND |
| 11 RTCK | 12 GND |
| 13 TDO  | 14 GND |
| 15 nRST | 16 GND |
| 17 TxDO | 18 GND |
| 19 RxDO | 20 GND |



MCU Power Selector



F/W DownLoad



LOGO1

Title: **A\_Link Cortex-M Debug Interface**Size: **A4**Number: **\***Revision: **Rev 1.2**

Date: 2021-12-17(수) Time: 오후 12:16:47

Sheet: \* of \*

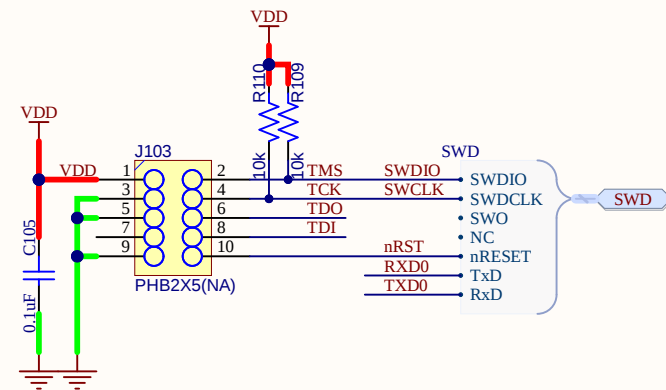
File: **A\_Link.SchDoc**

ABOV Semiconductor Co., Ltd.  
93-lo, gag-li 1,  
OChang-eub, CheongWon-gu,  
Cheongju-si, Chungbuk,  
Korea (363-885)



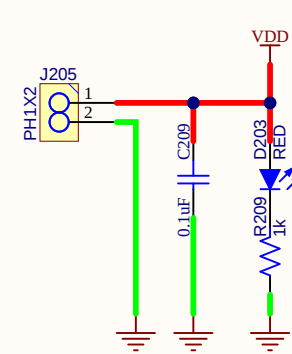
We recommend using X-tal Load capacitor value.

**CLOCK**

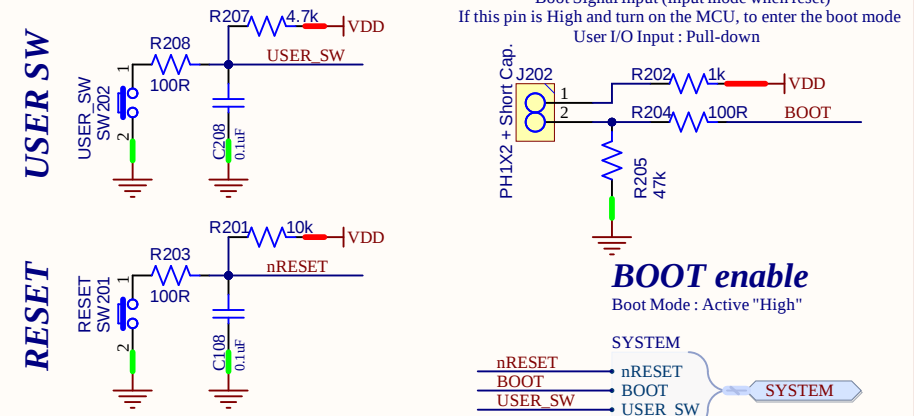


(SWCLK-Pull up, SWDIO-Pull up)

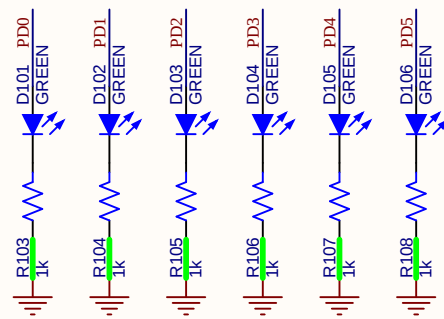
## Cortex Debug Connector (SWD)



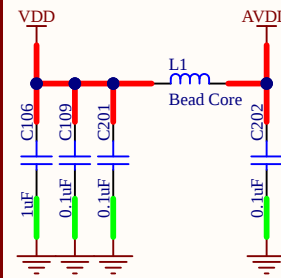
**POWER**



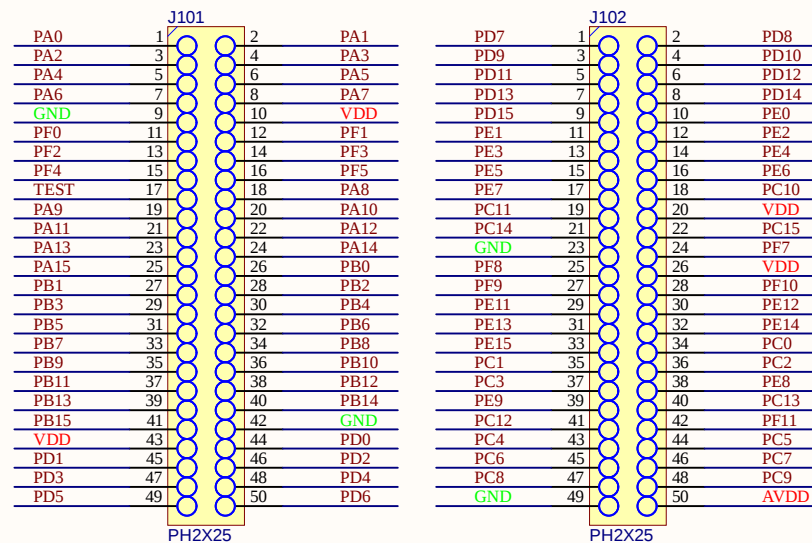
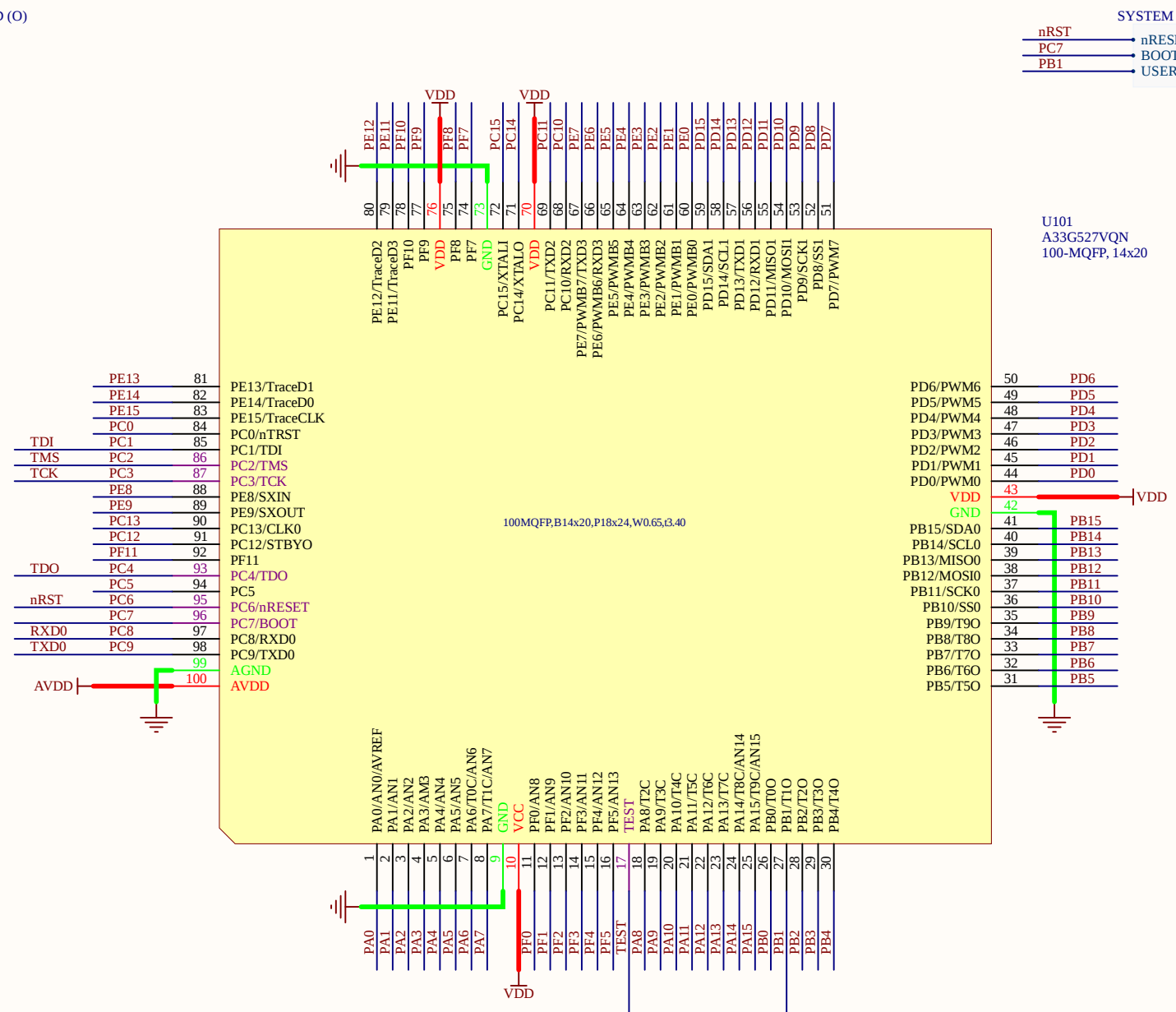
△ C208,C204 : Remove when using as user I/O port



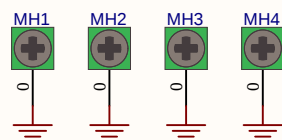
## PWM LED



*Bypass Cap.*



## USER IO



## MOUNTING HOLE

