Revision history #1

Use ABOV New S/W Version rule (2016. 3.18.Fri ~)

Version	Date	Description
V1.081.04	2022. 9.15.Thu	Fixed : - A96G140 USART2 Tx interrupt enable bit IE1.2 -> IE1.1
V1.081.03	2022. 8.16.Tue	Fixed : - A96R717/725/739 Interval timer setting ITDRL -> ITCRL
V1.081.02	2022. 7.18.Mon	Fixed : - A96F6832/6632 Timer3 PWM period
V1.081.01	2022. 6.27.Mon	Added device(s) : - A96G150 Added STK(s) : - A96G150 STK Fixed : - A96G166 SFR name P1DB -> P12DB - STK sample : variable type
V1.081.00	2022. 4.29.Fri	New feature : - Generate STK (StartKit) example code directly Added STK(s) : - A96G140 STK - A96G166 STK - A96G174 STK - A96G181 STK
V1.080.04	2022. 4. 6.Wed	Fixed : - A96G166 : SFR name fixed In UART 0, 1 read / write function SFR name USTAT, UDATA to U0STAT, U1STAT, U0DATA, U1DATA
V1.080.03	2022. 3.11.Fri	Fixed : - A96R717 : P0IO, P3PU address - Remove XSFR definition warning during Multiple

		source linking by compiler
V1.080.02	2021.11.10.Wed	Fixed : - A96T418 : UART1 TX (IE1.2 -> IE1.1) - Menu string change (KEIL <-> IAR)
V1.080.01	2021. 8.27.Fri	Fixed : - A94B114 : Timer2 (T1ADRH/L -> T2ADRH/L)
V1.080.00	2021. 7.28.Wed	New feature : - **Support KEIL only → Support IAR too** - Change device header file format to support both of KEIL and IAR - Change XDATA SFR definition to volatile unsigned char type Fixed : - A96G166 : U1STAT address - A96F6432 : Clock setting bug
V1.070.01	2021. 3.18.Thu	Fixed : - A96G166 : P1SFRL (T2o, PWM2o)
V1.070.00	2021. 1.18.Mon	Fixed : - A94B114 : Header (DPL/H address) - A96G166 : Header (port) - A96G174 : Clock setting - A97C450 : Clock setting (Authority SFR) - MC96F6432 : Clock setting (add SubXTAL) - SPI : Polarity - Timer : Ext. clock edge selection (A96G140, A96G166, A96G174) - PWM function : add OneShot/Repeat - USART : I2C, SPI UART → Group (A96G140, A96G166, A96G174) - WDT function : WDTRC clock - And so on Added devices(s) - A96G181
V1.060.01	2020. 2.18.Tue	Fixed : - A96R717 : Header file (R5 ~ 7) - A96R717 : Package, pin assignment (P20~23)

V1.060.00	2019.11.28.Thu	Fixed : - A96T336 : Set TS_CON.1 before SFR write - A96L312 : Line I/F 12bit Added device(s) : - A96L322 - A96L523
V1.059.00	2019. 9. 5.Thu	Fixed : SFR address / name - MC93F5516 (SPI_SL_CONF2) - MC95FT081 (WDT) - MC96F1206 (WDT) - MC97C450 (P1IO) Added device(s) : - A96T316 - A96T336 - A96T418 - A96G166 - A96G174
V1.058.00	2019. 2.15.Fri	Fixed : LCD bias SFR: - A96R717 - A96R739 Added device(s) : - A96G140 - A96R725
V1.057.00	2018.11.12.Mon	Fixed : - I2C (I2CCR or I2CMR) : reset SFR bit
V1.056.02	2018.10.16.Tue	Fixed : Timer interrupt masking: - MC95FG308 : Timer1 - MC96F6432 : Timer4 - MC96F7864 : Timer8 - MC97FG316 : Timer1 - MC97F66128/68128/60128 : Timer8 Remove device(s) : - MC97F66128A/68128A
V1.056.01	2018.10. 4.Thu	Change device name: - MC97F66128 → MC97F66127 - MC97F66128A → MC97F66128

V1.056.00	2018. 9.20.Thu	Added device(s) : - A96R150
V1.055.00	2018. 8.22.Wed	Added device(s) : - A96L302
V1.054.00	2018. 7.16.Mon	Added device(s) : - A94E114 - A96T356 - MC96FE316
V1.053.03	2018. 6.26.Tue	Fixed : - A94B114 : LVI/LVR SFR setting
V1.053.02	2018. 4. 3.Tue	Fixed : Device configuration - MC96F8104/8204 memory map Code : 8KB → 4KB XDATA : 256B → 0B Memory model : Large → Small
V1.053.00	2018. 2.28.Wed	Added device(s) : - A96T346
V1.052.00	2018. 2. 7.Fri	Added device(s) : - A96R136 Fixed : - MC96FR364C Ext. INT port selection
V1.051.00	2017.12.22.Fri	Added device(s) : - A96R739 Add a code : - A96R717 interval timer
V1.050.00	2017.10.10.Tue	Added device(s) : - A96L312
V1.049.00	2017. 5.15.Mon	Added device(s) : - A94B114 Fixed : - It displayed empty “func_def.h” but file saving was OK
V1.048.04	2017. 4.10.Mon	Fixed : - SCCR access needs permission : MC94F1202A

		- Timer enable bit was not generated at PWM, Capture : MC94F1202A/1206 : MC97F1204S/1316S/2208H/8324H
V1.048.03	2017. 4. 3.Mon	Fixed : - MC97F6x128 : P46DB setting
V1.048.02	2017. 3.15.Wed	Add code - MC96F6432 : MC96F6432A only XTAL filter SFR Change : - MC97F6x128(A) : startup.a51 Include LCD RAM area to XDATA clear range Fixed : - MC97F60128 : P50 secondary function names P50/SEG8/RxD4 -> P50/SEG18/RxD4
V1.048.01	2017. 3. 8.Wed	Fixed : - MC96F6432 : P2SFRL MOSI1 mismatch - MC94F1202A : header file (Flash SFR address)
V1.048.00	2017. 2.14.Tue	Added device(s) : - A97C450
V1.047.01	2017. 1.17.Tue	Fixed : - Devices : MC97F6108A, MC97F6208 - SFR writing sequence (High byte first) - Timer, PWM, PPG
V1.047.00	2016. 8.18.Thu	Added device(s) : - A96R717
V1.046.01	2016. 7. 4.Mon	Fixed : - MC96F7848C : Watchdog timer setting sequence Insert WDTIDR setting before WDTCR setting - MC97FG316 : SFR address T3PPR: 0xFF -> 0xCB - MC96F8204 : SFR name TnXXX -> T1XXX, T2XXX
V1.046.00	2016. 5.17.Tue	Added device(s) : - MC96F8204 New feature : - Support Package view zoom-in/out

		Fixed : - MC94F1202A SCCR clock divisor value - MC96FT1616 Timer4 used Timer1 configuration
V1.045.01	2016. 3.18.Fri	Fixed : - MC96F6509 Timer4 used Timer1 configuration
V1.045.00	2015.12.24.Thu	Added device(s) : - MC97F68128A
V1.044.00	2015.12.11.Fri	Added device(s) : - MC96FR364C
V1.043.00	2015.11.23.Mon	Added device(s) : - MC97F6208 Fixed : - MC97FG316 SFR address (datasheet error) WDTC, WDTSR (0x2014~15) -> 0x2F14~15 Modification : - Device : MC97F6108A - Add Comparator code generation - Fixed : Timer clock & capture input source. - Remove OP-Amp code generation. Because of, the OP-Amp is too complex and requires too many conditions, it could not generate standard code.
V1.042.00	2015.11. 9.Mon	Added device(s) : - MC96FM408
V1.041.00	2015.10. 5.Mon	Added device(s) : - MC95FT081 Modification : - Modify device header (XDATA SFR) - Add "extern" for Multi-source Fixed : - 96F083 did not generate Timer1 code
V1.040.00	2015. 9.21.Mon	Added device(s) : - MC96F7848C Modification : - Modify device header (XDATA SFR) - Declare "#define" to "unsigned char XDATA"

		Fixed : - 96F6832 port9 SFR (P9CDR) option - 96F7064 port SFR P1DB missing

Revision history #2

Before use ABOV New S/W Version rule

Version	Fixed item	Contents
V1.0.37	Fixed : Timer setting ● MC94F1202A ● MC97F1316/6108A/8324H	Using external source. PWM clock selection.
V1.0.35	Fixed : Code & XDATA area setting ● startup.a51 ● UV2 project	
V1.0.34	Ext. interrupt #10~17 polarity : SFR value ● MC96F7864/7664 VLC pin name error ● MC96F7864/7664	SFR (EIPOL2L, EIPOL2H) P70~73 (VCL3~0 -> VLC3~0)
V1.0.31	ADC trigger missing ● MC96FT241 Port selection error ● MC96F6408/6509	 SFR (P5FSRH : TxD)
V1.0.30	Following device's Touch SFR (RSD) value ● MC96FT1616/242 IRC 125KHz division error ● MC96FT1616/241	 IRC 125KHz division is not prepared
V1.0.29	96FM204 Ext. OSC change	Ext. OSC SFR OSCCR.0 -> OSCCR.1
V1.0.26	Following device's watch timer SFR (WTDR) is write only ● MC96F6332/6432/6508A/6509/6632/6832/7816/7864/8316 ● MC97F2664/60128	"WTDR |= 0x80;" was invalid.
V1.0.24	Timer symbol error ● MC96F6108A	Change SFR name. T1DR -> T1DRH
V1.0.23	header file error ● MC96FT241/242/1616	Change SFR (FETCR) address 0xE -> 0xED
V1.0.21	header file error ● MC96FR332B/364B	Change SFR (P3) address 0x9F -> 0xC0

Device list

Series	Devices			
A94	A94B114			
A96	A96G140 A96G181 A96L302 A96L523 A96R136 A96R717	A96G150 A96L306 A96R150 A96R725	A96G166 A96L312 A96R739	A96G174 A96L322
A97	A97C450			
MC93	93F5516			
MC94	94F1202A			
MC95	95FG0128 95FG208 95FR332 95FT081	95FG6128 95FG308 95FR364	95FG8128 95FR432	 95FR464
MC96	96F1206 96F4548 96F5126 96F6332 96F6408A 96F6509 96F6632 96F7064 96F7416A 96F7616T 96F7664 96F7848C 96F8204 96F8208S 96FB504 96FC664A 96FD316 96FM204 96FM408	 96F5216A 96F6432 96F6508A 96F6832 96F7616A 96F7816 96F7864 96F8126 96FC864A 96FM214	 96F5416 96F8316	 96F5416A

	96FR116C 96FR3128 96FR332A 96FR364B 96FT083 96FT1602 96FT1702 96FT241 96FT242 96P0202 96P1102 96P6408	 96FR4128 96FR364C 96FT084 96FT1604 96FT1703 96FT161 96FT202 96P6608	 96FT085 96FT1608 96FT1704 96FT162	 96FT1616
MC97	97F1104 97F1316 97F2208H 97F2464 97F60128 97F66128A 97F6108A 97F6208 97F8324H 97FG316	97F1204 97F2664 97F66128 97F68128A	97F1215 97F67128	97F1216 97F68128